PATENT S/N Unknown

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Gilroy J. Vandentop et al.

Serial No .:

Unknown

Herewith

Filed: Title:

Group Art Unit: Unknown

Docket: 884.540US1

Examiner: Unknown

ELECTRONIC PACKAGE HAVING MULTIPLE-ZONE INTERCONNECTS ANI

METHODS OF MANUFACTURE

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 et. seq., the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of the 1449 form, initialled by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Please charge any additional fees or credit any overpayment to Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

GILROY J. VANDENTOP ET AL.

By their Representatives,

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Date of Deposit: November 30, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the US Patent and Trademark Office, Box Patent Application, P.O. Box 2327, Arlington, VA 22202.

Sheet 1 of 1

Form 1449*

Atty. Docket No.: 884.540US1

Serial No. Unknown

Applicant: Gilroy J. Vandentop et al.

BY APPLICANT
(Use several sheets if necessary)

Filing Date: Herewith

Group: Unknown

U.S. PATENT DOCUMENTS							
xaminer nitial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
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	_ 6,219,241 B1			361	704	06/11/99	
		FC	REIGN PATENT DOCUMEN	TS			
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nitial	Document Number	2000		*			
Examiner Initial	(Including Author, Title, Date, Pertinent Pages, Etc.) Ma, L., et al., "Compliant Cantilevered Spring Interconnects for Flip-Chip						
	Packaging" (May 2001)	, <u>2001 Electro</u>	onic Components and T	echnology	Conference	<u>ce</u> , 6 pages,	
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	Naeemi, A., et al., "Sea of Leads: A Disruptive Paradigm for a System-on-a-Chip (SoC)", <u>ISSCC 2001/Session 17/TD: 3D Technologies and Measurement Techniques/17.7</u> , 280-281, (Feb. 2001)						
	Reed, H.A.	, et al., "Co	ompliant Wafer Level ds (SoL) Interconnect	Package (CWLP) With	n Embedded 151-153. (Ju	

Examiner	Date Considered

^{*}Substitute Disclosure Statement Form (PTO-1449)

^{**}EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.